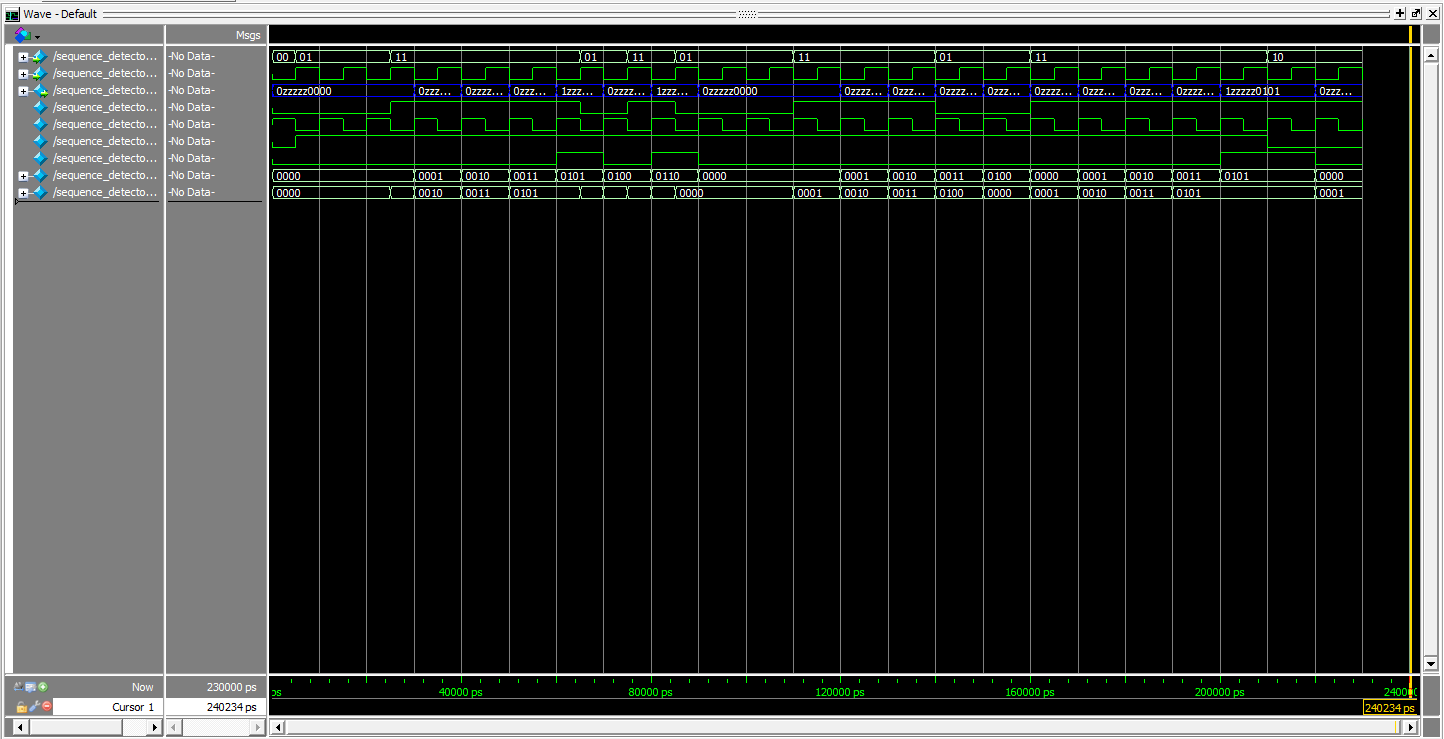
Part I



Clock

Z (LEDR[9])

W (SW[1])

{W, Reset}

Reset (sync)

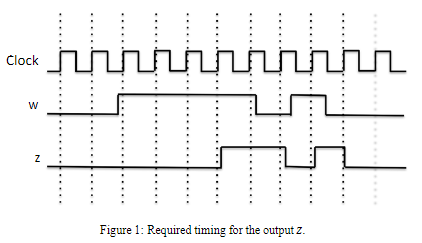
A to F

D to E

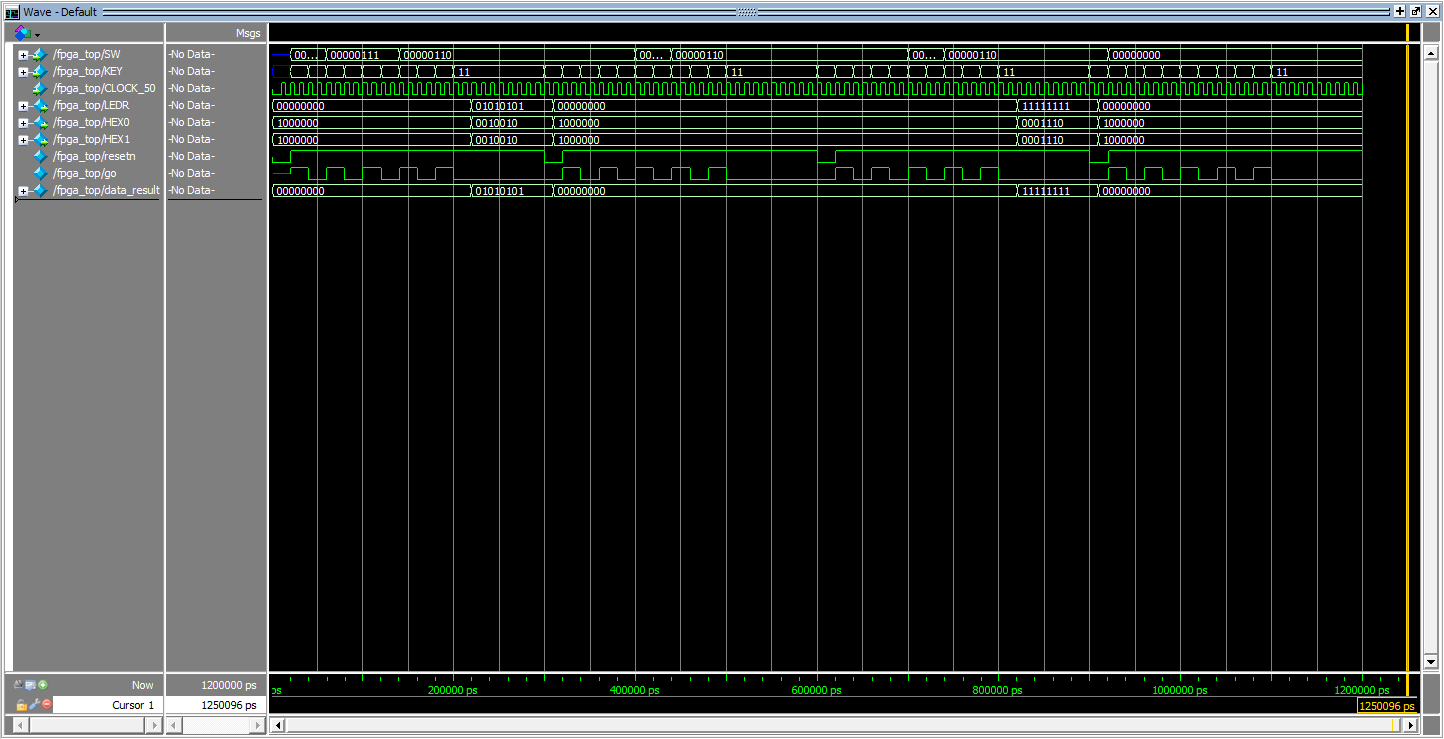
then

E to A

A to D



Part II



Answer

A=0, B=0, C=0, X=0

Ans=0=7’b0

A=6, B=6, C=3, X=6

Ans=255=7’b11111111

A=6, B=6, C=4, X=6

Ans=256=8’b100000000

=7’b0

A=1, B=7, C=7, X=6

Ans=85=7’b01010101

RTL Schematic

